Title (en)

VARIABLE DELAY CIRCUIT

Publication

EP 0244991 A3 19891018 (EN)

Application

EP 87303608 A 19870424

Priority

GB 8610888 A 19860503

Abstract (en)

[origin: EP0244991A2] A data processing system is described comprising a display terminal (10) and a processing unit (11). The display terminal includes a video timing generator (14) producing synchronisation signals (VSYNC, HSYNC). This triggers requests (QUAL) for the processing unit to supply video data. The display terminal includes a variable delay circuit (24) which measures the time delay between the outgoing request and the incoming data, and causes the synchronisation signals to be delayed by a corresponding amount. This ensures that the synchronisation signals are maintained in the correct timing relationship with the video data, irrespective of any unknown delays between the display terminal and the processing unit.

IPC 1-7

G09G 1/00

IPC 8 full level

G09G 5/12 (2006.01)

CPC (source: EP)

G09G 5/12 (2013.01)

Citation (search report)

- [X] US 3887769 A 19750603 - CICHETTI JR MICHAEL PETER, et al
- [X] GB 2073515 A 19811014 - INT STANDARD ELECTRIC CORP
- [YD] EP 0175564 A2 19860326 - INT COMPUTERS LTD [GB]
- [A] GB 2128450 A 19840426 - HITACHI LTD
- [XP] EP 0180450 A2 19860507 - RCA CORP [US]
- [X] PATENT ABSTRACTS OF JAPAN vol. 5, no. 82 (E-59)(754) 29 May 1981; & JP-A-56 030 369 (TOKYO SHIBAURA DENKI K.K.) 26.03.1981
- [X] PATENT ABSTRACTS OF JAPAN vol. 9, no. 85 (E-308)(1808) 13 April 1985; & JP-A-59 216 334 (NIPPON DENSHIN DENWA KOSHA) 06.12.1984

Cited by

US11744342B2

Designated contracting state (EPC)

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DOCDB simple family (publication)

EP 0244991 A2 19871111; **EP 0244991 A3 19891018**; GB 8610888 D0 19860611

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