

Title (en)

A multiport memory and source arrangement for pixel information.

Title (de)

Multi-Port-Speicher und Quelleneinrichtung für Bildpunktinformation.

Title (fr)

Mémoire à multiples portes et source pour information de points d'image.

Publication

EP 0245564 A1 19871119 (EN)

Application

EP 86400976 A 19860506

Priority

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Abstract (en)

The present system includes, in a preferred embodiment, a plurality of bit map memory units which together define a large bit map memory. For each bit map memory unit there is also included a mask means and four extended shift registers. The shift registers can be loaded in parallel with pixel information through bidirectional data transmission channels which include bidirectional mask means. The pixel information can be routed through said bidirectional mask means to different address locations, or to the same address location, with certain of the pixel bits removed by the mask means. The shift registers have both serial and parallel input and output means and are clocked at different speeds to accommodate different peripherals. At least a first shift register is designed to be serially read out at a relatively high rate which can be advantageously used by a video display device or the like. Information signals from the other shift registers are transferred at high speed (in parallel) into and out of the large bit map memory to said first shift register whereby pixel information signals are settled down before being routed from said first shift register. The bidirectional mask means and the bidirectional data transmission channels along with the multiplicity of shift registers permit the present system to handle many varied operations which operate at different speeds.

IPC 1-7

G09G 1/16

IPC 8 full level

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CPC (source: EP)

G09G 5/346 (2013.01); **G09G 5/39** (2013.01); **G09G 5/36** (2013.01)

Citation (search report)

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- [A] US 4174536 A 19791113 - JACOBSEN ROBERT G [US], et al
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