

Title (en)

Testing circuit for random access memory device.

Title (de)

Prüfschaltung für eine Speichereinrichtung mit willkürlichem Zugriff.

Title (fr)

Circuit d'essai pour des dispositifs de mémoire à accès direct.

Publication

EP 0253161 A1 19880120 (EN)

Application

EP 87109030 A 19870624

Priority

JP 15034786 A 19860625

Abstract (en)

In a semiconductor random access memory device of the type having two or more data lines arranged in association with a single data input or output terminal is provided a memory testing circuit which is characterized in that test data is supplied to every one of the data lines and is written all at a time into a plurality of memory cells which may include those located adjacent each other, wherein the number of the memory cells into which test data is to be written simultaneously depends on the data lines to be selected so that different pieces of data can be respectively written into the individual memory cells. A portion of an address signal is used not for the selection of the memory cells during the test data write cycle of the testing operation but for controlling the inversion of the test data to be written into selected ones of the memory cells and is supplied to the memory cells associated with any one or more of the data lines, whereby pieces of data complementary to each other can be supplied to the adjacent memory cells respectively through two of the data lines, providing a basis on which an interference test can be conducted for the memory cells located adjacent each other.

IPC 1-7

G11C 29/00; **G11C 11/00**; **G01R 31/28**; **H01L 21/66**

IPC 8 full level

G11C 29/00 (2006.01); **G11C 11/401** (2006.01); **G11C 11/409** (2006.01); **G11C 29/34** (2006.01)

CPC (source: EP US)

G11C 29/34 (2013.01 - EP US)

Citation (search report)

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Designated contracting state (EPC)

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DOCDB simple family (application)

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