

Title (en)

Digital timing signal generator and voltage regulator circuit.

Title (de)

Digitalimpulssignalgenerator und Spannungsreglerkreis.

Title (fr)

Générateur de signaux d'impulsions numériques et circuit régulateur de tension.

Publication

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Application

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Priority

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Abstract (en)

A digital timing signal generator and voltage regulator circuit is provided. In one embodiment the circuit includes a delay line. The delay line operating voltage is derived from digitally encoded power/timing signals transmitted by an isolated logic control circuit. The delay line receives and propagates the digitally encoded signals. Outputs of selected stages of the delay line are tapped to provide multiphasic timing signals for use by associated logic circuits. A plurality of gates having inputs connected to various stages of the delay line receive selected timing signals as they propagate along the delay line. Increases in the operating voltage cause the selected timing signals to sequentially activate the gates. The output of each activated gate then goes high and current flows through an associated load resistor connected between the output of the gate and ground to continuously load the supply voltage and thereby regulate it. In variations of this embodiment, two and three levels of gates and load resistors are provided to progressively load the supply voltage and thereby provide additional regulation thereof. In another embodiment, a ring-oscillator comprised of CMOS inverters generates the timing signals. The ring oscillator consumes current in approximately a square relationship with increases in its supply voltage and thereby regulates the voltage.

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