

Title (en)

Control of the program counter used in a pipelined computer.

Title (de)

Steuerung des Befehlszählers in einem Rechner mit Fließbandverarbeitung.

Title (fr)

Contrôle du compteur d'instruction dans un ordinateur pipe-line.

Publication

**EP 0265972 B1 19950222 (EN)**

Application

**EP 87116007 A 19871030**

Priority

JP 25986686 A 19861030

Abstract (en)

[origin: EP0265972A2] A processor capable of processing a variable word length instruction has a program counter controlled to indicate the head of an instruction by the value of the program counter. There are provided an adder for summing the length of decoded portions in the variable word length instruction in accordance with the progress of the instruction decoding, and another adder for adding the length of the decoded instruction portions to the program counter so as to update the program counter. Further, there is provided an circuit for calculating an operand effective address by using the value of the program counter in the course of the variable word length instruction decoding. Thus, the updating of the program counter and the generation of the effective address are concurrently executed.

IPC 1-7

**G06F 9/32**

IPC 8 full level

**G06F 9/30** (2006.01); **G06F 9/32** (2006.01); **G06F 9/355** (2006.01); **G06F 9/38** (2006.01)

CPC (source: EP)

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