

Title (en)
DISPLAY SYSTEM OF PLASMA DISPLAY.

Title (de)
PLASMA-ANZEIGESYSTEM.

Title (fr)
SYSTEME DE VISUALISATION DE PLASMA.

Publication
EP 0266429 A4 19890412 (EN)

Application
EP 87902718 A 19870410

Priority
JP 9540386 A 19860424

Abstract (en)
[origin: EP0266429A1] A system comprises a CPU (1), a ROM (2) storing a control program, a character RAM (3), a character generator (4), a graphic RAM (5), a synthesising circuit (6), a plasma display (10) with X- and Y-axis drivers (12,14), a shift register (11), an address generator (13) and a timing generating circuit (15). Data stored in the RAM's (3,5) are transferred serially to the shift register (11). When the data transfer is finished, a signal (W,END) is given to the timing generating circuit which then outputs a signal (BUSY) to prohibit further data transfer as well as a signal (HSYNC) to prompt the data writing onto the plasma display (10).

IPC 1-7
G09G 3/28; **G09G 3/36**

IPC 8 full level
G09G 3/28 (2006.01); **G09G 3/288** (2006.01); **G09G 3/296** (2013.01)

CPC (source: EP)
G09G 3/296 (2013.01)

Citation (search report)

- [X] US 4266225 A 19810505 - BURNETT BRADLEY W, et al
- [Y] EP 0108516 A2 19840516 - SHARP KK [JP]
- [A] EP 0121070 A2 19841010 - IBM [US]
- [A] EP 0162605 A1 19851127 - SONY CORP [JP]
- See references of WO 8706755A1

Designated contracting state (EPC)
DE FR GB

DOCDB simple family (publication)
EP 0266429 A1 19880511; **EP 0266429 A4 19890412**; JP S62251792 A 19871102; WO 8706755 A1 19871105

DOCDB simple family (application)
EP 87902718 A 19870410; JP 8700227 W 19870410; JP 9540386 A 19860424