

Title (en)  
Logic voting-circuit.

Title (de)  
Logische Abstimmuschaltung.

Title (fr)  
Circuit voteur logique.

Publication  
**EP 0266811 A1 19880511 (EN)**

Application  
**EP 87201872 A 19870930**

Priority  
NL 8602636 A 19861021

Abstract (en)  
The invention relates to a logic circuit having a plurality (N) inputs, the amount of which is at least three ( $N \geq 3$ ), said inputs being adapted to be supplied with binary input signals, and having an output supplying a binary output signal, the value of which equals the majority of the values of the input signals. The mentioned prior art system has, particularly in case of fail-safe circuits, of which an extreme reliability is required, the disadvantage that the voting-mechanism is present only in a single fashion, and therefore is a potentially vulnerable part in a total safe-guarding-chain. The invention now proposes to provide a logic circuit of the type mentioned in the preamble with a number (N) and AND-gates, the number (N) corresponding to the number (N) of inputs, of the magnetic type, each having a magnetizable element, e.g. a ring core, a first input connected with a writing winding cooperating with said element, a second input connected with a reading winding cooperating with said element, and an output connected with a detection-winding cooperating with said element, said inputs of the AND-gates being connected with a corresponding input of the circuit, in which the first input of an AND-gate (1, 2 ..., N-1, 1) is connected with the second input of the next AND-gate (2, 3 ..., N, 1), and the outputs of all AND-gates being connected with the output of the circuit.

IPC 1-7  
**H03K 19/23**; **H03K 19/16**

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**H03K 19/16** (2006.01); **H03K 19/23** (2006.01)

CPC (source: EP US)  
**H03K 19/16** (2013.01 - EP US); **H03K 19/23** (2013.01 - EP US)

Citation (search report)  
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• [A] US 3832566 A 19740827 - GERRY M  
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