Title (en)

METHODS AND APPARATUS FOR GIVING ACCESS TO INSTRUCTIONS IN COMPUTER SYSTEMS

Publication

EP 0270310 A3 19911127 (EN)

Application

EP 87310479 A 19871127

Priority

US 93619386 A 19861201

Abstract (en)

[origin: EP0270310A2] Methods and apparatus are set forth for optimizing the performance of instruction processors using an instruction cache memory in combination with a sequential transfer main memory. According to the invention, the novel memory system stores preselected instructions in cache memory. The instructions are those that immediately follow a branch operation. The purpose of storing these instructions is to minimize, and if possible, eliminate the delay associated with fetching the same sequence from main memory following a subsequent branch to the same instruction string. The number of instructions that need to be cached (placed in cache memory) is a function of the access time for the first and subsequent fetches from sequential main memory, the speed of the cache memory, and instruction execution time. The invention is particularly well suited for use in computer systems having RISC architectures with fixed instructions lengths.

IPC 1-7

G06F 9/38

IPC 8 full level

G06F 12/08 (2006.01); **G06F 9/38** (2006.01)

CPC (source: EP US)

G06F 9/3808 (2013.01 - EP US)

Citation (search report)

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