

Title (en)
TRI-STATE OUTPUT CIRCUIT

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Application
EP 88105267 A 19880331

Priority
JP 7647487 A 19870331

Abstract (en)
[origin: EP0285157A2] A tri-state output circuit comprising an input section (I) having complementary field effect transistors (P1,N1,P2,N2;P3N3) which constitute NOR gate (1) and invertor circuits (2), a control section (II) having first and second current control circuits (5,6) and an output section (III) having bipolar transistors (Q1,Q2,Q3,Q4) wherein an input signal and a tri-state signal are logically processed in the input section (I) and its result applied to the control section (II). Then, the switching operations of the output section (III) and a high impedance condition of the output terminal of the tri-state output circuit are controlled by the control section (II) consisting of a plurality of complementary FETs (P4,N5), thereby achieving a low power consumption, a high load driving capability, and a high speed operation.

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IPC 8 full level
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CPC (source: EP KR US)
H03K 19/09429 (2013.01 - EP US); **H03K 19/09448** (2013.01 - EP US); **H03K 19/20** (2013.01 - KR)

Citation (search report)
• [X] DE 3506265 A1 19850829 - HITACHI LTD [JP]
• [A] ELEKTRONIK, vol. 34, no. 4, 22nd February 1985, pages 93-97, Munich, DE; P. MAUGEST: "Fortschritte bei transistorisierten Brückenschaltungen"
• [A] IBM TECHNICAL DISCLOSURE BULLETIN, vol. 27, no. 4B, September 1984, page 2325, IBM Corp., New York, US; S.S. RUSSELL: "Power integrated switching darlington with speed-up capacitor"

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