Title (en)

MEMORY CONTROL SYSTEM

Publication

EP 0289899 A3 19901010 (EN)

Application

EP 88106592 A 19880425

Priority

US 4645687 A 19870504

Abstract (en)

[origin: EP0289899A2] A system for controlling the addressing of a memory on a predetermined multi-megabyte decode boundary. An address shifter is coupled between CPU address lines and backplane area bussed address lines. The address shifter is controlled in accordance with the control signal determined by the memory array of largest capacity of all memory arrays. The control signal has different states to control the address shifter to couple different address bit patterns therethrough to the backplane area address bus as a function of the selected control signal state.

IPC 1-7

G06F 12/06

IPC 8 full level

G06F 12/06 (2006.01)

CPC (source: EP US)

G06F 12/0661 (2013.01 - EP US); **G06F 12/0684** (2013.01 - EP US)

Citation (search report)

- [A] EP 0200198 A2 19861105 - DIGITAL EQUIPMENT CORP [US]
- [A] US 4281392 A 19810728 - GRANTS VALDIS, et al
- [A] IBM TECHNICAL DISCLOSURE BULLETIN, vol. 11, no. 1, June 1968, pages 67-70, New York, US; L.R. PALOUNEK: "Memory allocation and addressing"

Cited by

EP0398727A3; EP0782077A1; GB2234095A; GB2234095B

Designated contracting state (EPC)

AT BE CH DE ES FR GB GR IT LI LU NL SE

DOCDB simple family (publication)

EP 0289899 A2 19881109; **EP 0289899 A3 19901010**; AU 1418788 A 19881110; AU 612636 B2 19910718; CA 1305562 C 19920721; JP S63285650 A 19881122; US 4888687 A 19891219

DOCDB simple family (application)

EP 88106592 A 19880425; AU 1418788 A 19880405; CA 564206 A 19880414; JP 9802588 A 19880420; US 4645687 A 19870504