Title (en)

REGISTER

Publication

EP 0298747 A3 19891115 (EN)

Application

EP 88306230 A 19880707

Priority

IT 2120187 A 19870707

Abstract (en)

[origin: EP0298747A2] In the register an applied data signal (D) or its complement (D) is used to set or reset an output RS flip-flop (13) under control of an applied load control signal (L). The load control signal is applied to a switching circuit (12,14) which controls application of the data signal (D, D) to the set or reset input of the output flip-flop (13') such that the data signal is only applied for a time period sufficient to cause a change in state of the output flip-flop (13').

IPC 1-7

H03K 3/037; G11C 11/34

IPC 8 full level

H03K 3/037 (2006.01)

CPC (source: EP KR US)

G06F 12/00 (2013.01 - KR); **H03K 3/037** (2013.01 - EP US)

Citation (search report)

- [Y] US 4607173 A 19860819 - KNOEDL JR GEORGE [US]
- [X] IEEE TRANSACTIONS ON COMPUTERS, vol. C-22, no. 5, May 1973, pages 524-531, IEEE, New York, US; J.G. BREDESON et al.: "Synthesis of multiple-input change asynchronous circuits using transition-sensitive flip-flops"
- [Y] IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, vol. IM-21, no. 2, May 1972, pages 148-153; I.P. MACFARLANE: "Pulse generator and flip-flops"

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Designated contracting state (EPC)

AT BE CH DE ES FR GB IT LI NL SE

DOCDB simple family (publication)

EP 0298747 A2 19890111; **EP 0298747 A3 19891115**; AU 1877888 A 19890112; AU 602991 B2 19901101; BR 8803391 A 19890124; IL 86977 A0 19881230; IT 1221969 B 19900831; IT 8721201 A0 19870707; JP H01164114 A 19890628; KR 890002768 A 19890411; US 4893028 A 19900109; ZA 884805 B 19890329

DOCDB simple family (application)

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