

Title (en)

Semiconductor memory device with redundant memory cell array.

Title (de)

Halbleiterspeichergerät mit redundanter Speicherzellenmatrix.

Title (fr)

Dispositif de mémoire à semi-conducteur avec réseau de cellules de mémoire redondant.

Publication

**EP 0300467 A2 19890125 (EN)**

Application

**EP 88111715 A 19880720**

Priority

JP 18161287 A 19870720

Abstract (en)

There is disclosed a semiconductor memory device comprising a plurality of major memory cell blocks (32 to 39) divided into a plurality of sub-blocks (40 to 71), a redundant memory cell block (74) identical in size with each sub-block, write-in/sense amplifier circuits (118 to 126), two stages of selectors (76 to 108 and 109 to 116) operative to transfer data bits supplied from the respective major memory cell blocks and the redundant memory cell block to the write-in/sense amplifier circuits, a redundant information storage (136) for storing memory locations of defective major memory cells in one of the major memory cell block, and a shifting circuit (127) operative to replace the data bit read out from one of the defective major memory cells with the data bit read out from the redundant memory cell block on the basis of the memory location stored in the storage, and the number of the write-in/sense amplifier circuits is equal to the total number of the major memory cell blocks and the redundant memory cell block, so that the write-in/sense amplifier circuits consume a relatively small amount of area by virtue of the reduction in number.

IPC 1-7

**G06F 11/20**

IPC 8 full level

**G11C 29/00** (2006.01); **G11C 29/04** (2006.01)

CPC (source: EP US)

**G11C 29/848** (2013.01 - EP US)

Cited by

US5471427A; EP0549193A3; EP0499131A1; EP0434200A1; EP0401957A3; US5379258A; EP0856793A3; EP0858032A3; EP0858033A3; EP1197864A3; GB2251101A; GB2251101B; EP0412838A3; US5157628A

Designated contracting state (EPC)

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