

Title (en)
CMOS reference voltage generating device.

Title (de)
CMOS-Referenzspannungsgenerator.

Title (fr)
Générateur de tension de référence CMOS.

Publication
EP 0301184 A1 19890201 (EN)

Application
EP 88107309 A 19880506

Priority
US 7236287 A 19870713

Abstract (en)
A reference voltage generating device includes a first (Q1) and second (Q2) identical FET devices coupled in a parallel configuration with a biasing network of FET devices, interconnecting the substrate terminal of the first FET device to a first reference voltage VBs between a positive voltage supply (VDD) and ground potential. The control terminal of the first FET device (Q1) is connected to a second reference voltage (VACG) different from the first reference. The substrate terminal of the second FET device (Q2) is connected to its source terminal. The source terminals of both FET devices are connected to the respective input terminals of an operational amplifier (10) whose output is connected to the control terminal of said second FET device (Q2).

IPC 1-7
G05F 3/24

IPC 8 full level
G05F 3/24 (2006.01)

CPC (source: EP US)
G05F 3/245 (2013.01 - EP US)

Citation (search report)

- [A] US 4454467 A 19840612 - SAKAGUCHI JIROH [JP]
- [A] GB 2093303 A 19820825 - CITIZEN WATCH CO LTD
- [AD] EP 0014149 A1 19800806 - COMMISSARIAT ENERGIE ATOMIQUE [FR]

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EP0785494A3; EP0451870A3; EP0382929A3; US5029282A; US8933684B2; WO9931801A1; WO9506905A1; TWI484316B

Designated contracting state (EPC)
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DOCDB simple family (application)
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