

Title (en)
VIDEO DISPLAY INTERFACE

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EP 0304484 A4 19901227 (EN)

Application
EP 88903523 A 19880315

Priority
US 2590487 A 19870316

Abstract (en)
[origin: WO8807250A2] A video display interface adapted for use with D.C. electroluminescent display panels and constant current display drivers is disclosed. The video display interface receives serial video data at a frame rate of 60 Hz, converts it into eight bit words and stores it in a double-buffered video memory according to a memory map having ten sections corresponding to ten logical display sections. The video display interface reads stored video data out of the memory map, converts it to ten bit parallel output words and outputs the ten bit words to display drivers to drive multiple sections of the display simultaneously at an output frame rate of 240 Hz. The video display interface also generates constant current and pre-charge control signals that are used by the display drivers to generate constant current and pre-charge signals for driving the display.

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G09G 3/30

IPC 8 full level
G09G 3/30 (2006.01)

CPC (source: EP KR)
G09G 3/30 (2013.01 - EP KR); **G09G 2310/0251** (2013.01 - EP)

Citation (search report)
• [A] US 4193095 A 19800311 - MIZUSHIMA MASASHI [JP]
• [A] 1984 SID INTERNATIONAL SYMPOSIUM, DIGEST OF TECHNICAL PAPERS, 1984, pages 242-244, Palisades Institute for Research Services, Inc., New York, US; T. GIELOW et al.: "Multiplex drive of a thin-film EL panel"
• [XP] 1987 SID INTERNATIONAL SYMPOSIUM, DIGEST OF TECHNICAL PAPERS, 1987, pages 295-298, Palisades Institute for Research Services, Inc., New York, US; D. CHANNING et al.: "Drive system for a 600*200 DCEL display"
• See references of WO 8807250A2

Designated contracting state (EPC)
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