Title (en)

SERIAL INTERFACE

Publication

EP 0304813 A3 19910410 (DE)

Application

EP 88113485 A 19880819

Priority

DE 3728793 A 19870828

Abstract (en)

[origin: EP0304813A2] 1.1 Circuit arrangement for evaluating control signals 2.1 In highly integrated data processors, the number of control ports is restricted. There is a problem to supply different control signals via the existing control ports. 2.2 In a circuit arrangement for evaluating control signals output from a data processor, which consists of static and dynamic control signals, a memory is provided to which the static control signals are supplied and another memory is provided which is synchronised by the dynamic signal. 2.3 The circuit arrangement can be applied in the processing of control signals in a receiver for digital audio broadcasting.

IPC 1-7

H04H 5/00; H04J 3/04

IPC 8 full level

H04B 1/16 (2006.01); **H04H 20/88** (2008.01); **H04H 40/18** (2008.01); **H04J 3/04** (2006.01)

CPC (source: EP)

H04H 40/90 (2013.01)

Citation (search report)

- [A] GB 2150793 A 19850703 - MATSUSHITA ELECTRIC WORKS LTD
- [A] GB 2164526 A 19860319 - YAMATAKE HONEYWELL CO LTD

Designated contracting state (EPC)

AT BE CH DE ES FR GB GR IT LI LU NL SE

DOCDB simple family (publication)

EP 0304813 A2 19890301; **EP 0304813 A3 19910410**; **EP 0304813 B1 19931027**; AT E96589 T1 19931115; DE 3728793 A1 19890309; DE 3885204 D1 19931202; HK 124494 A 19941118; JP 2950834 B2 19990920; JP S6471338 A 19890316

DOCDB simple family (application)

EP 88113485 A 19880819; AT 88113485 T 19880819; DE 3728793 A 19870828; DE 3885204 T 19880819; HK 124494 A 19941110; JP 21086788 A 19880826