Title (en)

DOUBLE BUFFERED GRAPHICS DESIGN SYSTEM

Publication

EP 0312720 A3 19900613 (EN)

Application

EP 88112554 A 19880802

Priority

US 11090287 A 19871020

Abstract (en)

[origin: EP0312720A2] A graphic display system comprises a video display controller including two similar frame buffer memories for alternatively receiving and storing incoming pixel data and for periodically refreshing a display on a screen selectively in accordance with pixel data stored by either one of the two frame buffer memories. While the video display controller periodically refreshes the screen display in accordance with the pixel data stored in a first of the frame buffer memories, incoming pixel data is stored in the second frame buffer memory. The video display controller begins periodically refreshing the screen display in accordance with the pixel data stored in the second frame buffer memory. Updated pixel data stored in the second frame buffer memory is then copied into the first frame buffer memory.

IPC 1-7

G09G 1/16; G09G 1/28

IPC 8 full level

G06F 3/153 (2006.01); **G06T 11/00** (2006.01); **G09G 5/399** (2006.01)

CPC (source: EP)

G09G 5/399 (2013.01)

Citation (search report)

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