

Title (en)

CURRENT CONFINEMENT AND BLOCKING REGION FOR SEMICONDUCTOR DEVICES

Publication

**EP 0314372 A3 19891025 (EN)**

Application

**EP 88309770 A 19881019**

Priority

US 11491087 A 19871029

Abstract (en)

[origin: EP0314372A2] Improved current confinement and current blocking are achieved in a semiconductor device including a doped (n or p type) semiconductor layer (32) within a region of high resistivity semiconductor material (31,33). In another embodiment, a plurality of doped semiconductor layers are interleaved with a plurality of high resistivity semiconductor layers.

IPC 1-7

**H01S 3/19**

IPC 8 full level

**H01L 33/00** (2010.01); **H01L 33/14** (2010.01); **H01L 33/30** (2010.01); **H01S 5/00** (2006.01); **H01S 5/227** (2006.01); **H01S 5/22** (2006.01)

CPC (source: EP)

**H01S 5/227** (2013.01); **H01S 5/2224** (2013.01); **H01S 5/2226** (2013.01); **H01S 5/2227** (2013.01); **H01S 5/2275** (2013.01)

Citation (search report)

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- [A] EP 0208209 A2 19870114 - NEC CORP [JP]
- [Y] PATENT ABSTRACTS OF JAPAN

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Designated contracting state (EPC)

DE FR GB NL SE

DOCDB simple family (publication)

**EP 0314372 A2 19890503; EP 0314372 A3 19891025;** JP H01146390 A 19890608

DOCDB simple family (application)

**EP 88309770 A 19881019;** JP 26838788 A 19881026