

## Title (en)

Power high election mobility structure.

## Title (de)

Hochelektronengeschwindigkeits-Leistungstransistorstruktur.

## Title (fr)

Structure de transistor de puissance, à haute mobilité électronique.

## Publication

**EP 0314877 A1 19890510 (DE)**

## Application

**EP 88111246 A 19880713**

## Priority

US 8375187 A 19870807

## Abstract (en)

A modulating-doped field effect transistor comprises a substantially undoped channel layer (10), a n-doped wide bandgap donor layer (12) and a relatively heavily doped cap layer (14). It further comprises a gate recess (17) through a top insulating layer (16), having a cross-section in the cap layer (14) increasing down to the interface with the donor layer (12) and thereafter having a cross-section in said donor layer (12) decreasing down to the bottom of the recess (12) in said donor layer. A Schottky gate electrode (24) which does not occupy the portions of the recess (17) in the undercut part is formed in said recess (17) using the insulating layer (16) as a shadow mask.

## IPC 1-7

**H01L 21/28; H01L 21/306; H01L 29/205; H01L 29/64; H01L 29/80**

## IPC 8 full level

**H01L 29/812** (2006.01); **H01L 21/285** (2006.01); **H01L 21/306** (2006.01); **H01L 21/335** (2006.01); **H01L 21/338** (2006.01); **H01L 29/423** (2006.01); **H01L 29/778** (2006.01)

## CPC (source: EP US)

**H01L 21/28587** (2013.01 - EP US); **H01L 21/30621** (2013.01 - EP US); **H01L 29/42316** (2013.01 - EP US); **H01L 29/66462** (2013.01 - EP US); **H01L 29/7787** (2013.01 - EP US)

## Citation (search report)

- [A] FR 2168936 A1 19730907 - LABO ELECTRONIQUE PHYSIQUE [FR]
- [A] IEEE ELECTRON DEVICE LETTERS, vol. EDL-4, no. 9, September 1983, pages 306-307, IEEE, New York, US; M.D. FEUER et al.: "High-speed low-voltage ring oscillators based on selectively doped heterojunction transistors"
- [A] PROCEEDINGS OF THE 4TH CONFERENCE ON SOLID STATE DEVICES, Tokyo, 1972, Supplement to the Journal of the Japan Society of Applied Physics, vol. 42, 1973, pages 78-87, Tokyo, JP; Y. TARUI et al.: "Self-aligned GaAs schottky barrier gate fet using preferential etching"
- [A] PATENT ABSTRACTS OF JAPAN, vol. 10, no. 236 (E-428)[2292], 15th August 1986; & JP-A-61 69 175 (NEC CORP.) 09-04-1986
- [A] IEEE ELECTRON DEVICE LETTERS, vol. EDL-5, no. 7, July 1984, pages 241-243, IEEE, New York, US; Y. TAKANASHI et al.: "Control of threshold voltage of AlGaAs/GaAs 2DEG FET's through heat treatment"

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DE FR GB NL

## DOCDB simple family (publication)

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## DOCDB simple family (application)

**US 8375187 A 19870807**; EP 88111246 A 19880713; JP 19429988 A 19880802