Title (en)

Delay circuits for integrated circuits.

Title (de)

Verzögerungsschaltungen für integrierte Schaltungen.

Title (fr)

Circuits de retard pour circuits intégrés.

Publication

EP 0315385 A2 19890510 (EN)

Application

EP 88310186 A 19881028

Priority

JP 27687487 A 19871031

Abstract (en)

A delay circuit includes a current mirror circuit having a pair of MOS transistors (11, 12), a constant current source (14) and a capacitance (16). The delay time of the circuit is determined by the charging time of the capacitance (16) connected to one (12) of the MOS transistors. A stable delay time may be obtained despite manufacturing fluctuations, and the occupation area of the circuit may be reduced.

IPC 1-7

G11C 19/18; H03K 5/13

IPC 8 full level

G11C 19/18 (2006.01); **H03H 11/26** (2006.01); **H03K 5/13** (2014.01); H03K 5/00 (2006.01)

CPC (source: EP US)

G11C 19/184 (2013.01 - EP US); **H03H 11/26** (2013.01 - EP US); **H03K 5/133** (2013.01 - EP US); H03K 2005/00195 (2013.01 - EP US)

Cited by

EP0405319A1; EP0493149A1; FR2671244A1; US5334891A; EP0493150A1; FR2671245A1; US5463343A

Designated contracting state (EPC)

DE FR GB IT

DOCDB simple family (publication)

EP 0315385 A2 19890510; **EP 0315385 A3 19900328**; **EP 0315385 B1 19940413**; DE 3889069 D1 19940519; DE 3889069 T2 19940728; JP H01119114 A 19890511; US 5006738 A 19910409

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EP 88310186 A 19881028; DE 3889069 T 19881028; JP 27687487 A 19871031; US 53786890 A 19900613