

Title (en)

Forcing synchronisation on two pulse trains.

Title (de)

Zwangsmässige Synchronisation zweier Impulsfolgen.

Title (fr)

Synchronisation forcée de deux trains d'impulsions.

Publication

EP 0318155 B1 19940511 (EN)

Application

EP 88310048 A 19881026

Priority

US 12166787 A 19871117

Abstract (en)

[origin: EP0318155A1] An apparatus and method for digital correction of oscillator drift provides for phase alignment between two clock signals (10, 12) running at nearly the same frequency. Phase alignment is provided by fashioning a delay for one of the clock signals through selection of various lengths (40) of a variable delay path (20) formed from a series of logic circuits. Respective reference signals are derived from the two clocks to be phase-aligned, and the phases of the references are compared in a digital phase comparator (14). The product of phase comparison controls a digital delay selector (18) to generate a sequence of delay signals corresponding to a sequence of detected phase differences. The delay signal sequence controls the variable digital delay. The variable digital delay outputs a corrected clock signal whose phase is aligned with the phase of the other clock signal. The corrected clock signal is used to produce one reference signal, the other reference signal being derived directly from the other clock signal. A second digital phase comparator (22) compares the phase of the corrected clock signal with a predetermined reference phase of the clock signal from which it is derived. When the phases of the clocks are aligned, the second comparator produces a reset signal which resets the digital selection circuit to a predetermined point in the delay signal sequence, thereby operating the variable digital delay to correct the clock signal to a phase corresponding to the predetermined reference phase. The use of digital circuitry to correct for drift between the two clock signals permits the invention to be fully embodied in integrated digital circuits. The elimination of requirement for any analog circuitry to correct for oscillator drift permits phase alignment at various points along the line of clock distribution in an integrated digital system. By use of the invention, phase alignment can be performed on-chip between discrete functions on a single integrated circuit, between separate integrated circuits, and between independently-operating digital systems.

IPC 1-7

H03L 7/00; H04L 7/04

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Cited by

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