Title (en)

DATA PROCESSING DEVICE

Publication

EP 0323140 A3 19910925 (EN)

Application

EP 88312184 A 19881222

Priority

JP 33371987 A 19871229

Abstract (en)

[origin: EP0323140A2] A data processing device having a buffer (3) for prefetching a plurality of instructions, the buffer (3) is constructed by including two switching areas (A, B) enabling a switching and one common area (C) connecting to one of the two switching areas (A, B), as unconnected switching area of the two switching areas (B, A) is used exclusively for prefetching a destination instruction of a conditional jump instruction, so that the destination instruction is prefetched to the unconnected switching area (B, A) by a switching operation, and thus flexibility is increased, when the jump instructions are continued. Further, a number of prefetching destination instructions is determined so that a bottleneck in an instruction process is avoided, and thus the capacity of the two switching areas (A, B) is reduced the hard ware scale is not enlarged.

IPC 1-7

G06F 9/38

IPC 8 full level

G06F 9/38 (2006.01)

CPC (source: EP KR US)

G06F 9/28 (2013.01 - KR); **G06F 9/381** (2013.01 - EP US)

Citation (search report)

- [A] US 3614747 A 19711019 - ISHIHARA KOICHIRO, et al
- [A] EP 0180725 A2 19860514 - IBM [US]
- [A] GB 2011682 A 19790711 - HONEYWELL INF SYSTEMS
- [A] IEEE TRANSACTIONS ON COMPUTERS, vol. C-32, no. 11, November 1983, pages 977-989, New York, US; Y. TAMIR et al.: "Strategies for managing the register file in RISC"

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EP0449368A3

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

EP 0323140 A2 19890705; **EP 0323140 A3 19910925**; **EP 0323140 B1 19961009**; DE 3855605 D1 19961114; DE 3855605 T2 19970213; JP H01175634 A 19890712; JP H0769812 B2 19950731; KR 890010695 A 19890810; KR 930000097 B1 19930108; US 4992932 A 19910212

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EP 88312184 A 19881222; DE 3855605 T 19881222; JP 33371987 A 19871229; KR 880017797 A 19881229; US 29033588 A 19881227