

Title (en)
A DATA PATH CHECKING SYSTEM

Publication
EP 0335510 A3 19910313 (EN)

Application
EP 89302129 A 19890303

Priority
GB 8807606 A 19880330

Abstract (en)
[origin: EP0335510A2] A data pathchecking system for resolving data transfer errors in a plane of directly connected switching elements, the system checking the plane of directly connected switching elements by designating one switching element with an associated control element as a master and other switching elements and associated control elements as slaves. The master switch element instructs other switch elements discretely to check their respective switching element for data transfer errors and checks its own switching element for data transfer errors. Furthermore, the master switch is arranged to validate connections between switching elements.

IPC 1-7
H04Q 11/04; **H04M 3/26**

IPC 8 full level
H04M 3/26 (2006.01); **H04Q 1/24** (2006.01); **H04Q 11/04** (2006.01)

CPC (source: EP KR US)
H04L 5/00 (2013.01 - KR); **H04M 3/303** (2013.01 - EP US); **H04Q 11/04** (2013.01 - EP US)

Citation (search report)
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• [Y] EP 0103083 A2 19840321 - CSELT CENTRO STUDI LAB TELECOM [IT]
• [A] FR 2463560 A1 19810220 - PLESSEY CO LTD [GB]
• [A] PROCEEDINGS OF THE NATIONAL ELECTRONICS CONFERENCE. vol. 36, 01 October 1982, OAK BROOK, ILLINOIS pages 175 - 180; J.L.Clements: "Network maintenance for a microprocessor controlled pulse code modulation telephone switching system"

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US5937032A; WO9720436A3

Designated contracting state (EPC)
BE DE ES FR GR IT LU NL SE

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EP 0335510 A2 19891004; **EP 0335510 A3 19910313**; AU 3175389 A 19891005; AU 615040 B2 19910919; CN 1016390 B 19920422; CN 1036674 A 19891025; DK 152089 A 19891001; DK 152089 D0 19890329; FI 891511 A0 19890329; FI 891511 A 19891001; GB 2219172 A 19891129; GB 2219172 B 19920708; GB 8807606 D0 19880505; JP H0213095 A 19900117; KR 890015532 A 19891030; PT 90166 A 19891110; US 5042038 A 19910820

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