

Title (en)
INPUT/OUTPUT CIRCUITS

Publication
EP 0335715 A3 19920325 (EN)

Application
EP 89303150 A 19890330

Priority
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Abstract (en)
[origin: EP0335715A2] An input/output circuit in which a plurality of data lines (BS) are provided with a serial/parallel conversion circuit (30) common to all the data lines (BS) so that the circuit consumes less power and draws a reduced instantaneous current during operation, and can also be fabricated in integrated circuit form. Switch means (33A1 to 33N4) connect the data lines (BS) with plural sets of unit data lines (LA to LN) in response to control means (37A to 37N), such that at least one set of the unit data lines (LA to LN) is sequentially turned on.

IPC 1-7
G11C 7/00

IPC 8 full level
G11C 7/10 (2006.01)

CPC (source: EP US)
G11C 7/10 (2013.01 - EP US); **G11C 7/103** (2013.01 - EP US)

Citation (search report)
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• [Y] ELECTRONICS LETTERS vol. 3, no. 6, June 1967, STEVENAGE, GB pages 282 - 283; P.M. CASHIN ET AL.: 'Time-division multiplexer/demultiplexer for digital transmission in the gigabit per second range'
• [A] J.E.E. JOURNAL OF ELECTRONIC ENGINEERING vol. 23, no. 233, May 1986, TOKYO, JP pages 66 - 70; A. TEZUKA ET AL.: 'GaAs logic IC enables development of ultrahigh-speed optical communications systems'
• [A] BBC RESEARCH DEPARTMENT REPORT no. 5, July 1987, TADWORTH, GB pages 1 - 20; J.L. RILEY: 'A review of the semiconductor storage of television signals: Part 1 Historical introduction and design philosophy'

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Designated contracting state (EPC)
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