

Title (en)
BIC MEMORY CELL STRUCTURE AND A MANUFACTURING METHOD THEREOF

Publication
EP 0336679 A3 19910925 (EN)

Application
EP 89303271 A 19890403

Priority
• JP 8274688 A 19880404
• JP 8274788 A 19880404

Abstract (en)
[origin: EP0336679A2] A BIC memory cell device comprises a first insulating layer (25) covering a MOS structure (T1), a first penetrating opening (26) in the first insulating layer in correspondence to a drain region (22) and defined by an inclined first side wall (26c) which defines the diameter of the first opening such that the diameter increases towards a top surface of the first insulating layer, a second penetrating opening (28) in the first insulating layer in correspondence to a source region (21) and defined by a second side wall (28a) having a straight vertical cross section, a third penetrating opening (29) in the first insulating layer in correspondence to a gate electrode (23) and defined by a third side wall (29a) having a straight vertical cross section, a second insulating layer (27) provided on the first insulating layer in correspondence to the drain region, a first wiring electrode (31) deposited such that the second insulating layer is sandwiched between the first wiring electrode and the drain region, and second and third wiring electrodes (32, 33) contacting with the source region and the gate electrode.

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H01L 27/10; **H01L 21/82**; **G11C 17/00**

IPC 8 full level
G11C 17/00 (2006.01); **H01L 21/768** (2006.01); **H10B 20/00** (2023.01); **H10B 69/00** (2023.01)

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G11C 17/00 (2013.01 - EP US); **H01L 21/76895** (2013.01 - EP US); **H10B 69/00** (2023.02 - EP KR US); **H01L 21/76895** (2013.01 - KR)

Citation (search report)
• [A] EP 0224418 A1 19870603 - FUJITSU LTD [JP]
• [A] PATENT ABSTRACTS OF JAPAN, vol. 11, no. 351 (E-557)[2798], 17th November 1987; & JP-A-62 130 559 (FUJITSU LTD) 12-06-1987

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US5968851A; EP0510604A3; US6373099B1

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