

Title (en)
CONTENT ADDRESSABLE MEMORY ARRAY ARCHITECTURE

Publication
EP 0341897 A3 19921028 (EN)

Application
EP 89304467 A 19890504

Priority
US 19331588 A 19880511

Abstract (en)
[origin: EP0341897A2] A content addressable memory system includes a plurality of memory cells arranged in rows and columns in an array of N bit words by M word cells, a plurality of word lines extending through the array for addressing different words in the memory cells, each of the words comprising a plurality of adjacent cells extending in a first direction in the array, a plurality of match lines extending through the array in parallel with the word lines in the first direction, a plurality of bit lines extending through the array in a second direction perpendicular to the first direction, each of the bit lines communicating with the cells in one of the columns extending in the second direction, and a pair of registers connected to the bit lines for performing masking operations on bits in the array.

IPC 1-7
G06F 15/40

IPC 8 full level
G06F 17/30 (2006.01); **G11C 15/04** (2006.01)

CPC (source: EP US)
G06F 16/90339 (2018.12 - EP US); **G11C 15/04** (2013.01 - EP US)

Citation (search report)

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- [A] PROCEEDINGS. VLSI AND COMPUTERS. FIRST INTERNATIONAL CONFERENCE ON COMPUTER TECHNOLOGY, SYSTEMS AND APPLICATIONS. COMP EURO 87. 15 May 1987, HAMBURG, GERMANY pages 19 - 26; WALDSCHMIDT: 'ASSOCIATIVE PROCESSORS AND MEMORIES, OVERVIEW AND CURRENT STATUS'
- [A] ELECTRONICS INTERNATIONAL vol. 51, no. 2, January 1978, pages 7 - 8; 'Associative processor on a chip due from British laboratory'
- [XP] ELECTRONIC DESIGN. vol. 36, no. 27, 8 December 1988, HASBROUCK HEIGHTS, NEW JERSEY pages 119 - 121; BURSKEY: 'CONTENT-ADDRESSABLE MEMORY DOES FAST MATCHING'

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