

Title (en)
METHOD OF PRODUCING SEMICONDUCTOR DEVICES

Publication
EP 0355799 A3 19910123 (DE)

Application
EP 89115504 A 19890823

Priority
DE 3828809 A 19880825

Abstract (en)
[origin: US5096844A] The invention relates to a method in particular for manufacturing bipolar transistors. By applying selective epitaxy methods and by using self-adjusting techniques, the process sequence is shortened and the transistor properties are improved.

IPC 1-7
H01L 21/82; **H01L 21/285**; **H01L 21/20**

IPC 8 full level
H01L 21/20 (2006.01); **H01L 21/285** (2006.01); **H01L 21/331** (2006.01)

CPC (source: EP US)
H01L 21/02381 (2013.01 - EP US); **H01L 21/02392** (2013.01 - EP US); **H01L 21/02395** (2013.01 - EP US); **H01L 21/02461** (2013.01 - EP US); **H01L 21/02463** (2013.01 - EP US); **H01L 21/02543** (2013.01 - EP US); **H01L 21/02546** (2013.01 - EP US); **H01L 21/02639** (2013.01 - EP US); **H01L 21/28525** (2013.01 - EP US); **H01L 29/66242** (2013.01 - EP US); **H01L 29/66287** (2013.01 - EP US); **Y10S 438/969** (2013.01 - EP US)

Citation (search report)

- [X] US 4663831 A 19870512 - BIRRITELLA MARK S [US], et al
- [A] EP 0189136 A2 19860730 - TOSHIBA KK [JP]
- [A] DE 3545238 A1 19870625 - LICENTIA GMBH [DE], et al
- [A] EP 0125943 A1 19841121 - BENDIX CORP [US]
- [A] US 4507853 A 19850402 - MCDAVID JAMES M [US]
- IBM TECHNICAL DISCLOSURE BULLETIN. vol. 26, no. 6, November 1983, NEW YORK US Seiten 3022 - 3024; F.S.J.LAI: "Dielectrically isolated CMOS structure fabricated by reverse trench process"

Cited by
EP0484066A1; US5587327A; EP0684639A1

Designated contracting state (EPC)
DE FR GB IT

DOCDB simple family (publication)
EP 0355799 A2 19900228; **EP 0355799 A3 19910123**; **EP 0355799 B1 19950405**; DE 3828809 A1 19900301; DE 58909155 D1 19950511; US 5096844 A 19920317

DOCDB simple family (application)
EP 89115504 A 19890823; DE 3828809 A 19880825; DE 58909155 T 19890823; US 39836889 A 19890824