

Title (en)

METHOD OF ERASING LIQUID CRYSTAL DISPLAY AND AN ERASING CIRCUIT

Publication

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Application

**EP 89900891 A 19881223**

Priority

- JP 8801308 W 19881223
- JP 33176487 A 19871225
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Abstract (en)

[origin: WO8906416A1] When the display is to be erased from active matrix-type liquid crystal display elements which have a source bus drive circuit (16) and a gate bus drive circuit (17), pixel signals for turning the pixels off are supplied in an amount of one line to the source bus drive circuit and, at the same time, a clear signal (CL) is given to a gate bus drive circuit (17) to apply a voltage simultaneously to all gate buses (151? to 15m?) to turn on the transistors (13) in all of the pixels. Provision is made of a power source holding circuit (22) for holding the power of the power source (V1?) supplied to the gate bus drive circuit (17) for a predetermined period of time even after the power source is turned off, and a voltage drop detect circuit (24) for detecting the turn-off of the power source. A clear signal (CL) is produced in response to the detect signal and is sent to the gate bus drive circuit (17). In response to the clear signal, the gate bus drive circuit supplies a voltage for turning on the transistors (13) of all pixels simultaneously to all of the gate buses to erase the display in a short period of time after the power source is turned off.

IPC 1-7

**G09G 3/36**

IPC 8 full level

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**G09G 3/3648** (2013.01); **G09G 3/3677** (2013.01); **G09G 3/3696** (2013.01); **G09G 2310/0245** (2013.01); **G09G 2330/02** (2013.01)

Citation (search report)

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- [Y] EP 0035382 A1 19810909 - FUJITSU LTD [JP]
- PATENT ABSTRACTS OF JAPAN vol. 12, no. 006 (P-653)9 January 1988 & JP-A-62 165 630 ( SEIKO EPSON CORP. ) 22 July 1987
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