Title (en)

Device and method for driving a liquid crystal panel.

Title (de)

Steuereinrichtung und -verfahren für eine Flüssigkristallanzeigetafel.

Title (fr)

Dispositif et méthode de commande d'un panneau d'affichage à cristaux liquides.

Publication

EP 0368572 B1 19950802 (EN)

Application

EP 89311397 A 19891103

Priority

- JP 28002988 A 19881105
- JP 32647288 A 19881223

Abstract (en)

[origin: EP0368572A2] A circuit for driving a liquid crystal panel using a plurality of source drivers includes two line memory circuits for transmitting color signals to the source drivers for odd-numbered, and even-numbered source lines respectively. Each of the line memory circuits of the first construction includes circuits (39b, 39r, 39g, 40b, 40r, 40g, 41, 42) for forming a digital color signal train arranged in an order according to a color order of the corresponding source lines upon receipt of analog color signals of the three colors in parallel, memories (43, 44) for storing the digital color signal train successively according to an address order, circuits (43, 44, 49, 51, 52) for alternately reading a memory area of a second half and a memory area of a first half of the respective memories, and circuits (46b, 46r, 46g, 47b, 47r, 47g, l 1b, l 1r, l 1g) for latching the read digital color signals in a prescribed order, converting the same to analog color signals of the three colors in parallel and transmitting the analog color signals to the corresponding source drivers. The source drivers include source drivers (33, 34) for the source lines of the first half and source drivers (35, 36) for the source lines of the second half, which are activated alternately. The line memory circuit of the second construction includes circuits for forming a first digital data train for a first gate line from the three color signals supplied in parallel, circuits for forming a digital data train for the odd-numbered source lines and a digital data train for the even-numbered source lines from the two digital data trains, memories for storing the digital data for the odd-numbered and for the even-numbered source lines by classifying the data into eight areas, i.e. areas for the first and second gate lines, the odd-numbered source lines of the first and second halves and the even-numbered source lines of the first and second halves, circuits for alternately reading the data of the areas of the first half and second half of the odd-numbered source lines for the first gate line, and at the same time alternately reading the data of the area of the first half and second half of the even-numbered source lines for the first gate line, then reading the data for the second gate line in the same order after the reading of the data for the first gate line, thereby forming a data train for the odd-numbered source lines and a data train for the even-numbered source lines, and circuits for forming thus parallel analog color signal trains supplied independently to the odd-numbered and even-numbered source lines, out of the read digital data trains.

IPC 1-7

G09G 3/36

IPC 8 full level

G09G 3/36 (2006.01)

CPC (source: EP KR)

G09G 3/36 (2013.01 - KR); **G09G 3/3607** (2013.01 - EP); **G09G 3/3611** (2013.01 - EP); **G09G 3/3688** (2013.01 - EP); G09G 3/3614 (2013.01 - EP); G09G 2310/0205 (2013.01 - EP); G09G 2310/0224 (2013.01 - EP); G09G 2310/0281 (2013.01 - EP); G09G 2310/0297 (2013.01 - EP)

Citation (examination)

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