

Title (en)  
COMPUTING MACHINE WITH HYBRID COMMUNICATION ARCHITECTURE

Publication  
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Application  
**EP 89906950 A 19890407**

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Abstract (en)  
[origin: WO8909967A1] A computer comprises a plurality of processor modules (1100-110N), each having at least first and second I/O connection interfaces (126, 130A, 130B, 130C, 130D), a processor (122) connected to those interfaces (126, 130A, 130B, 130C, 130D), and read-write memory (118) connected to the processor. The first I/O connection interface (126) of each processor module (1100-110N) is connected to a common bus (138). The second I/O connection interface (130A, 130B, 130C, 130D) of each processor module (1100-110N) is connected to a switch (150A, 150B, 150C, 150D), the switch (150A, 150B, 150C, 150D) being operative to connect the second I/O connection interface (130A, 130B, 130C, 130D) of a selected processor module (1100-110N) selectively to the second I/O connection interface (130A, 130B, 130C, 130D) of any other processor module (1100-110N). A controller (142) is connected to the bus (138) for receiving over the bus (138) data pertaining to a first processor module (1100-110N), which requires access to information, and to a second processor module (1100-110N), from which the required information is available, and for controlling the switch (150A, 150B, 150C, 150D) to allow the required information to be transmitted from the first processor module (1100-110N) to the second processor module (1100-110N).

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