Title (en)
   MEMORY DATA SYNTHESIZER

Publication
   EP 0379186 A3 19910306 (EN)

Application
   EP 90100952 A 19900117

Priority
   JP 901389 A 19890118

Abstract (en)
   [origin: EP0379186A2] A ROM part (24) of a character ROM (21) stores a plurality of font data. A display data RAM (9) simultaneously supplies a plurality of address signals to the character ROM (21) which is provided with a plurality of address decoders (25, 26). Respective address signals are decoded by the corresponding address decoders (25, 26), so that the font data corresponding to the address signals are read on the common bit lines (BL1 - BL l). Thus, the font data as read are synthesized on the common bit lines (Bl1 - BL l) as a logical sum.

IPC 1-7
   G09G 1/02; G09G 5/24

IPC 8 full level
   H04N 5/278 (2006.01); **G09G 5/22** (2006.01); **G09G 5/24** (2006.01); **H04N 5/445** (2011.01)

CPC (source: EP)
   G09G 5/222 (2013.01); **G09G 5/24** (2013.01)

Citation (search report)
   • [Y] EP 0136819 A2 19850410 - HITACHI LTD [JP]
   • [A] EP 0206695 A2 19861230 - FUJITSU LTD [JP]
   • [AP] WO 8906030 A1 19890629 - NCR CO [US]
   • [Y] IBM TECHNICAL DISCLOSURE BULLETIN vol. 24, no. 12, May 1982, pages 6250,6251, Armonk, US; P.A. BEAVEN et al.: "Generation of Characters"

Designated contracting state (EPC)
   DE FR GB

DOCDB simple family (publication)
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