Title (en)

FABRICATION METHOD OFASEMICONNDUCTOR HAVING A PLANARIZED SURFACE

Publication

EP 0388862 A3 19910102 (EN)

Application

EP 90105171 A 19900320

Priority

JP 6865689 A 19890320

Abstract (en)

[origin: EP0388862A2] A semiconductor device having a multi-level interconnection structure comprises one or more active devices (4, 5, 6a, 6b, 7, 8, 22, 23a, 23b), a substrate (1, 21) supporting the active device thereon, a first insulator layer (9, 38) provided so as to cover the substrate including the active devices, a first conductor pattern (13, 25) provided on the first insulator layer, a planarizing layer (16, 30) having a planarized top surface provided on the first insulator layer so as to bury the first conductor pattern underneath, a second insulator layer (31) provided on the planarized top surface of the planarizing layer, a contact hole (33) provided on the second insulator layer so as to expose a desired part of the first conductor pattern, and a second conductor pattern (34) provided on the second insulator layer in correspondence to the contact hole so as to fill the contact hole and so as to make a contact to the exposed part of the first conductor pattern, wherein an isolated region is provided on the substrate in correspondence to a part of the substrate underneath the contact hole such that the isolated region is projected from the first top surface of the substrate in correspondence to the contact hole. The isolated region causes a projection of the top surface of the first insulator layer in correspondence to a part which covers the isolated region such that the planarizing layer provided on the first insulator layer is eliminated from the part of the first insulator having the projecting top surface.

IPC 1-7

H01L 21/90; H01L 21/3105

IPC 8 full level

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CPC (source: EP KR US)

H01L 21/3105 (2013.01 - EP US); **H01L 21/76804** (2013.01 - EP US); **H01L 21/76819** (2013.01 - EP US); **H01L 23/522** (2013.01 - KR); **H01L 23/5226** (2013.01 - EP US); H01L 2924/0002 (2013.01 - EP US)

C-Set (source: EP US)

H01L 2924/0002 + H01L 2924/00

Citation (search report)

- [A] WO 8707979 A1 19871230 - LSI LOGIC CORP [US], et al
- [A] IEEE 4TH. VLSI MULTILEVEL INTERCONNECT CONFERENCE 16 June 1987, IEEE NEW YORK USA pages 61 - 77; C.H. TING ET.AL.: "PLANARISATION PROCESS USING SPIN-ON GLASS"

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DOCDB simple family (application)

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