

Title (en)

Circuit to automatically power down a CMOS device which is latched up.

Title (de)

Schaltkreis, um die Energieversorgung einer CMOS-Einrichtung automatisch abzuschalten im Fall eines "Latch up".

Title (fr)

Circuit pour couper automatiquement l'alimentation d'un dispositif CMOS en cas de "latch up".

Publication

EP 0391672 A1 19901010 (EN)

Application

EP 90303571 A 19900403

Priority

US 33542089 A 19890407

Abstract (en)

An integrated circuit protection device for resetting an integrated circuit (11) when latch-up occurs has switching means (14) connected in series with a current path (13) to selectively control the flow of current through the integrated circuit. Voltage comparison means (17) monitors changes in voltage which correspond to changes in the current flowing through the integrated circuit. The voltage comparison means operates cooperatively with storage means (15) to provide an output to control the switching means (14). When latch-up is detected, the output signal to the switching means causes it to restrict current flow through the integrated circuit.

IPC 1-7

G05F 3/20

IPC 8 full level

G05F 3/20 (2006.01)

CPC (source: EP)

G05F 3/205 (2013.01)

Citation (search report)

- [X] US 4109161 A 19780822 - IJIMA HIROSHI
- [A] US 4260909 A 19810407 - DUMBRI AUSTIN C, et al
- [A] EP 0202074 A1 19861120 - ADVANCED MICRO DEVICES INC [US]
- [A] EP 0175152 A2 19860326 - LATTICE SEMICONDUCTOR CORP [US]

Cited by

EP1811568A1; CN116430212A; DE102005059795A1; US7310211B2; WO2005119777A1; US7692906B2

Designated contracting state (EPC)

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