

Title (en)
CROSSTALK-SHIELDED-BIT-LINE DRAM

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Application
EP 90104690 A 19900313

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US 34096289 A 19890420

Abstract (en)
[origin: EP0393347A2] This invention relates to semiconductor memories and includes a sense amplifier architecture in which sensed data bit lines (e.g. BL2, BL2 min) are electrically isolated and shielded from their immediately adjacent active neighbors by utilization of non-selected bit lines (e.g. BL1, BL1 min and/or BL3, BL3 min) as an AC ground bus. In its simplest embodiment, shielded bit line (SBL) architecture includes two pairs of opposed bit lines (BL1, BL2; BL1 min , BL2 min) associated with a common sense amplifier (10). One of each of the bit line pairs is multiplexed into the sense amplifier and the other unselected bit line pair is clamped to AC ground to shield the selected bit line pair from all dynamic line-to-line coupling.

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IPC 8 full level
G11C 7/18 (2006.01); **G11C 11/401** (2006.01); **G11C 11/4097** (2006.01)

CPC (source: EP US)
G11C 7/18 (2013.01 - EP US); **G11C 11/4097** (2013.01 - EP US)

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