Title (en)

IC WITH MEANS FOR REDUCING ESD DAMAGE

Publication

EP 0397780 A4 19910918 (EN)

Application

EP 89902440 A 19890123

Priority

US 15155588 A 19880202

Abstract (en)

[origin: WO8907334A1] An integrated-circuit (IC) chip having means to prevent or mitigate damage from electrostatic discharge (ESD) employing a thick dielectric coating (20, 26) of insulative oxide between the surface of chip substrate and the metallization film (22) used to make contact with regions of the substrate (10). At least a portion of this layer (26) is formed at temperatures below 700 DEG C. The coating (20, 26) is sufficiently thick everywhere that its breakdown voltage is greater than the breakdown voltage of any junction (14) in the substrate (10). This assures that the breakdown caused by ESD will always occur in the junction (14), which is self healing, rather than in the dielectric coating (20, 26), where the damage could be permanent.

IPC 1-7

H01L 21/285; H01L 29/86

IPC 8 full level

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CPC (source: EP)

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C-Set (source: EP)

H01L 2924/0002 + H01L 2924/00

Citation (search report)

- [A] EP 0057024 A1 19820804 - PHILIPS NV [NL]
- [A] US 4435447 A 19840306 - ITO TAKASHI [JP], et al
- [A] ELECTRICAL OVERSTRESS/ELECTROSTATIC DISCHARGE SYMPOSIUM PROCEEDINGS, Philadelphia PA, 1984, pages 202-209; C.M. LIN et al.: "A CMOS VLSI ESD input protection device, DIFIDW"
- See references of WO 8907334A1

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

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DOCDB simple family (application)

US 8900257 W 19890123; CA 589539 A 19890130; EP 89902440 A 19890123; JP 50226889 A 19890123