

Title (en)
OUTPUT BUFFER FOR REDUCING SWITCHING INDUCED NOISE

Publication
EP 0398098 A3 19910724 (EN)

Application
EP 90108489 A 19900506

Priority
US 35550989 A 19890519

Abstract (en)
[origin: CA2017102A1] Attorney Docket No. NS013470 OUTPUT BUFFER FOR REDUCING SWITCHING INDUCED NOISE An output buffer for reducing switching induced noise in high speed integrated circuit devices incorporates a relatively small current carrying capacity secondary pulldown transistor element with the current path first and second terminal leads coupled in parallel with the current path first and second terminal leads of the primary pulldown transistor element. A separate pulldown delay resistance element of selected value is coupled in series between the control terminal leads of the secondary and primary pulldown transistor elements. The secondary pulldown transistor element control terminal lead is coupled in the output buffer to receive a signal propagating through the output buffer before the primary pulldown transistor element control terminal lead. A relatively small discharge current is therefore initiated from the output before turn on of the relatively large discharge current of the primary pulldown transistor element. The separate pulldown delay resistance element delays turn on of the primary pulldown transistor element a specified time delay after turn on of the secondary pulldown transistor element during transition from high to low potential at the output. As result ground bounce is divided into two spikes and the ground rise in potential is constrained to approximately one half that of conventional ground bounce levels. A secondary pullup transistor element with associated noise reduction components can similarly be used on the supply side to reduce Vcc droop.

IPC 1-7
H03K 19/0175; **H03K 19/20**

IPC 8 full level
H01L 21/339 (2006.01); **H01L 29/762** (2006.01); **H03K 5/1252** (2006.01); **H03K 17/16** (2006.01); **H03K 19/003** (2006.01); **H03K 19/0175** (2006.01)

CPC (source: EP KR US)
H03K 19/00 (2013.01 - KR); **H03K 19/00361** (2013.01 - EP US); **H03K 19/0175** (2013.01 - KR); **H03K 19/20** (2013.01 - KR)

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Designated contracting state (EPC)
DE FR GB IT NL

DOCDB simple family (publication)
US 4961010 A 19901002; CA 2017102 A1 19901119; DE 69028730 D1 19961107; DE 69028730 T2 19970320; EP 0398098 A2 19901122; EP 0398098 A3 19910724; EP 0398098 B1 19961002; JP H0329413 A 19910207; KR 0136775 B1 19980515; KR 900019385 A 19901224

DOCDB simple family (application)
US 35550989 A 19890519; CA 2017102 A 19900518; DE 69028730 T 19900506; EP 90108489 A 19900506; JP 12705690 A 19900518; KR 900007153 A 19900518