

Title (en)

Method of polishing semiconductor wafer.

Title (de)

Verfahren zum Polieren von Halbleiterplättchen.

Title (fr)

Procédé de polissage de plaquettes semi-conductrices.

Publication

EP 0403287 B1 19941005 (EN)

Application

EP 90306519 A 19900614

Priority

JP 15374889 A 19890616

Abstract (en)

[origin: EP0403287A2] A semiconductor wafer (12) is ground or polished to a desired thickness by pressing the wafer against a rotating turntable (13), characterised in that the semiconductor wafer is bonded to a plate (11), and a thickness-regulating member (15) whose surface is more resistant to polishing/grinding than the semiconductor wafer is arranged on the plate. By way of example, the thickness-regulating member comprises a silicon matrix and has a silicon oxide film at the surface.

IPC 1-7

H01L 21/00; **B24B 37/04**

IPC 8 full level

B24B 37/07 (2012.01); **H01L 21/304** (2006.01)

CPC (source: EP)

B24B 37/013 (2013.01)

Citation (examination)

- JP S6471663 A 19890316 - HITACHI CABLE
- PATENT ABSTRACTS OF JAPAN vol. 13, no. 244 (M-834)(3592) 07 June 1989 ; & JP-A-1 051 268; & JP-A-64 051 268

Cited by

EP0561532A3; CN105199610A; GB2275130A; GB2275130B; US5445996A; US5914275A; US5948205A

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