Title (en)

SYNAPTIC ELEMENT AND ARRAY

Publication

EP 0414888 A4 19920311 (EN)

Application

EP 90906014 A 19900309

Priority

US 32249089 A 19890310

Abstract (en)

[origin: WO9010977A1] An electronic circuit is disclosed having a sample/hold amplifier connected to an adaptive amplifier (10). A plurality of such electronic circuits (10a...10d) may be configured in an array of rows (30, 32) and columns (34, 36). An input voltage vector may be compared with an analog voltage vector (Vi) stored in a row or column of the array and the stored vector closest to the applied input vector may be identified and further processed.

IPC 1-7

H03K 3/02; G11C 27/02

IPC 8 full level

G06N 3/063 (2006.01); **G11C 15/04** (2006.01); **G11C 27/02** (2006.01)

CPC (source: EP)

G06N 3/063 (2013.01); **G11C 15/04** (2013.01); **G11C 27/02** (2013.01)

Citation (search report)

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- [A] US 4594560 A 19860610 - DINGWALL ANDREW G F [US], et al
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- [A] US 4565971 A 19860121 - BROOKSHIRE DANIEL A [US]
- [A] ELECTRONICS WEEK. vol. 58, no. 21, May 1985, NEW YORK US pages 25 - 26; ROSE: 'UV-write-enable memory enhances logic chips'
- See references of WO 9010977A1

Designated contracting state (EPC)

DE FR GB IT NL SE

DOCDB simple family (publication)

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