Title (en)

Logic compiler for design of circuit models.

Title (de)

Logik-Kompilator zum Entwurf von Schaltungsmodellen.

Title (fr)

Compilateur logique pour la conception de modèles de circuit.

Publication

EP 0416669 A2 19910313 (EN)

Application

EP 90202055 A 19900727

Priority

US 40324789 A 19890905

Abstract (en)

A logic compiler wherein verification of a generated circuit model is performed automatically by comparing the operation of the circuit model with that of a corresponding mathematical behavior model. A novel user interface and circuit model generation means enables the user to obtain, in real time, performance specifications on the circuit selected by the user as well as incurring other benefits.

IPC 1-7

G06F 15/60

IPC 8 full level

G06F 17/50 (2006.01)

CPC (source: EP US)

G06F 30/30 (2020.01 - EP US); **G06F 30/33** (2020.01 - EP US); **G06F 30/3308** (2020.01 - US)

Cited by

US5377122A; US6152612A; EP0508075A3

Designated contracting state (EPC)

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EP 0416669 A2 19910313; **EP 0416669 A3 19930505**; **EP 0416669 B1 19980909**; DE 69032640 D1 19981015; US 5377122 A 19941227

DOCDB simple family (application)

EP 90202055 A 19900727; DE 69032640 T 19900727; US 14741993 A 19931101