

Title (en)
Process for fabricating high performance BiMOS circuits

Title (de)
Verfahren zur Herstellung von BiMOS-Schaltungen mit hoher Leistung

Title (fr)
Procédé pour la fabrication de circuits BiMOS de haute performance

Publication
EP 0418670 B1 19970319 (EN)

Application
EP 90117264 A 19900907

Priority
US 40954589 A 19890919

Abstract (en)
[origin: EP0418670A2] A method of making complementary vertical bipolar transistors and complementary field effect transistors on the same substrate is described. The process includes forming buried layers in a semiconductor substrate which are spaced apart in a self-aligned manner by use of a lateral etching technique to undercut the mask used for definition of the buried layers. In the process, the collector and base contacts of the bipolar devices and the corresponding conductivity-type sources and drains of the field effect transistors are combined to minimize processing steps. The process also includes a silicided polycrystalline silicon layer used to form resistors and contact the various transistors.

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H01L 21/82; **H01L 21/033**; **H01L 21/74**; **H01L 21/3205**

IPC 8 full level
H01L 21/02 (2006.01); **H01L 21/033** (2006.01); **H01L 21/74** (2006.01); **H01L 21/8222** (2006.01); **H01L 21/8249** (2006.01); **H01L 27/06** (2006.01); **H01L 27/10** (2006.01)

CPC (source: EP KR US)
H01L 21/033 (2013.01 - EP US); **H01L 21/74** (2013.01 - EP US); **H01L 21/8249** (2013.01 - EP US); **H01L 27/08** (2013.01 - KR); **H01L 28/20** (2013.01 - EP US); **Y10S 148/009** (2013.01 - EP US)

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DE FR GB IT NL

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EP 0418670 A2 19910327; **EP 0418670 A3 19920415**; **EP 0418670 B1 19970319**; DE 69030225 D1 19970424; DE 69030225 T2 19971030; JP 3220450 B2 20011022; JP H03270068 A 19911202; KR 100196483 B1 19990615; KR 910007133 A 19910430; US 5079177 A 19920107

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