

Title (en)
PIPELINE ARCHITECTURE FOR GENERATING VIDEO SIGNAL

Publication
EP 0419125 A3 19920812 (EN)

Application
EP 90310010 A 19900913

Priority
US 41107689 A 19890922

Abstract (en)
[origin: EP0419125A2] A symbol generator with pipeline architecture comprised of a series of processing stages that regenerate a complete video data signal for each display field is disclosed herein. The pipeline design offers a number of advantages over other systems. Any symbol in a display may be moved in real time and independently of any other symbol, because the display is regenerated for each and every field. The symbol generator includes a cpu microprocessor, vertical sorter, boundary generator, horizontal sorter, and color palette.

IPC 1-7
G09G 1/16; **G09G 5/24**; **G09G 5/06**

IPC 8 full level
G09G 5/06 (2006.01); **G09G 5/24** (2006.01); **G09G 5/42** (2006.01); **H04N 5/262** (2006.01)

CPC (source: EP)
G09G 5/24 (2013.01); **G09G 5/42** (2013.01)

Citation (search report)

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