

Title (en)
SIGNAL PIPELINING IN SYNCHRONOUS VECTOR PROCESSOR

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Application
EP 90311266 A 19901015

Priority
• US 42147189 A 19891013
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• US 42149489 A 19891013

Abstract (en)
[origin: EP0422963A2] A synchronous vector processor SVP device (102) having a plurality of one-bit processor elements (150) organized in a linear array. The processor elements are all controlled in common by a sequencer, a state machine or a control circuit (controller) (128) to enable operation as a parallel processing device. Each processor element (150) includes a set of input registers (154), two sets of register files (158,166), a set of working registers (162), an arithmetic logic unit (164) including a one-bit full adder/subtractor, and a set of output registers (168). In video applications each processor element (150) operates on one pixel of a horizontal scan line and is capable of real-time digital processing of video signals. Included within the SVP device is input circuitry enabling pipelining of address, data and control signals. The circuitry includes a plurality of latches (1452) and signal coding and decoding circuitry (1440,1448).

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G06F 15/80

IPC 8 full level
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Citation (search report)
• [A] EP 0317218 A2 19890524 - TEXAS INSTRUMENTS INC [US]
• [A] US 3566366 A 19710223 - QUINN THOMAS M, et al
• [A] IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS vol. CAS34, no. 11, November 1987, NEW YORK US pages 1375 - 1384 T. C. HENDERSON ET AL 'A pipelined architecture for parallel image relaxation operations'
• [A] THE 13TH ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE 2 May 1986, TOKYO pages 338 - 345 A. L. FISHER 'Scan line array processors for image computation'
• [A] IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE vol. 31, 17 February 1988, NEW YORK US pages 158 - 159 J. P. NORSWORTHY 'A parallel image processor chip'
• [AP] IEEE TRANSACTIONS ON CONSUMER ELECTRONICS vol. 36, no. 3, August 1990, NEW YORK US pages 318 - 325 H. MIYAGUCHI 'Digital tv with serial video processor'

Cited by
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