Title (en)

Semiconductor package with ground plane.

Title (de)

Halbleiterpackung mit Erdungsfläche.

Title (fr)

Empaquetage pour semi-conducteur avec conducteur de masse.

Publication

EP 0425775 A1 19910508 (EN)

Application

EP 90114931 A 19900803

Priority

US 42853389 A 19891030

Abstract (en)

A plastic encapsulated semiconductor package (42) in which the connecting lead frame members (10) are deposited over the surface of the device (14) together with a covering ground plane (12) so as to provide enhanced electrical and thermal coupling of the members and the device and so reduce the signal to noise ratio by a factor of greater than three over that available in other similar plastic encapsulated packages while simultaneously improving the transfer of heat out of the package. In particular, a lead frame having a plurality of conductors is attached to a major active surface of a semiconductor chip via a ground plane which, in the preferred embodiment, is a multilayered structure containing an insulated integral, uniform ground plane positioned between the lead frame and the chip and adhesively and insulatively joined to both of them. Wires connect terminals on the major active surface of the semiconductor chip to the ground plane and to selective lead frame conductors. The lead frame, the ground plane structure, the semiconductor chip, and the wires which connect the semiconductor chip terminals to the ground plane and to selected lead frame conductors are encapsulated with a suitable insulating material to form a semiconductor module or package.

IPC 1-7

H01L 23/495

IPC 8 full level

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CPC (source: EP US)

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Citation (search report)

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- [A] PATENT ABSTRACTS OF JAPAN vol. 13, no. 386 (E-812) 25 August 1989, & JP-A-01 134958 (HITACHI LTD) 26 May 1989,

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DOCDB simple family (application)

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