

Title (en)
IMPROVED PAGED MEMORY CONTROLLER

Publication
EP 0427425 A3 19920527 (EN)

Application
EP 90311650 A 19901024

Priority
US 43167089 A 19891103

Abstract (en)
[origin: EP0427425A2] A computer system has a processor (20) coupled to a cache controller (24), uses page mode memory devices (58) sand performs page hit detection (43) on the processor local bus (26). Column address and data values are latched by a memory controller (62) on memory write operations to allow early completion of the cycle so that the next cycle can partially overlap. This allows the use of economical memories and yet have zero wait state page hit operation.

IPC 1-7
G06F 12/08

IPC 8 full level
G06F 12/02 (2006.01); **G06F 12/08** (2006.01)

CPC (source: EP US)
G06F 12/0215 (2013.01 - EP US); **G06F 12/0882** (2013.01 - EP US)

Citation (search report)

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- [X] GB 2217066 A 19891018 - INT COMPUTERS LTD [GB]
- [Y] US 4621320 A 19861104 - HOLSTE DANIEL D [US], et al
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Designated contracting state (EPC)
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DOCDB simple family (publication)
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DOCDB simple family (application)
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