Title (en)
BIASING SCHEME FOR IMPROVING LATITUDES IN THE TRI-LEVEL XEROGRAPHIC PROCESS

Publication
EP 0429309 A3 19911106 (EN)

Application
EP 90312719 A 19901122

Priority
- US 44091389 A 19891122
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Abstract (en)
[origin: EP0429309A2] The operating latitude of the tri-level xerographic process is improved by replacing the standard DC bias that is applied to one or both of the developer housings (32, 34) in conventional tri-level imaging with a chopped DC (CDC) developer bias (41, 43). Chopped DC biasing is the alternate application of two discrete bias voltages to a developer strucrute in a periodic fashion at a given frequency, with the period of each cycle divided up between the two bias levels at a duty cycle of from 5-10% or 90-95% depending upon which of the two developer structures is being biased. In the case of the DAD developer structure (32) the duty cycle of the higher of the two biases is 5-10% and in the case of a CAD developer structure (34) the duty cycle of the higher of the two biases is 90-95%. The apparatus can be switched to operate in a black monochrome mode, in which only the black developer structure (34) is biased using a standard momchrome bias (4-5).

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G03G 15/01

IPC 8 full level
G03G 13/01 (2006.01); **G03G 15/01** (2006.01)

CPC (source: EP US)
G03G 13/013 (2013.01 - EP US); **G03G 15/0121** (2013.01 - EP)

Citation (search report)
- [YD] EP 0320277 A2 19890614 - XEROX CORP [US]
- [YP] EP 0378440 A2 19900718 - CANON KK [JP]
- [A] GB 2145942 A 19850411 - KONISHIROKU PHOTO IND
- [Y] PATENT ABSTRACTS OF JAPAN vol. 13, no. 242 (P-880)(3590) June 7, 1989 & JP-A-1 044 468 (FUJI XEROX) February 16, 1989

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DE FR GB

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