

Title (en)  
PARALLEL STRING PROCESSOR AND METHOD FOR A MINICOMPUTER

Publication  
**EP 0441873 A4 19920930 (EN)**

Application  
**EP 89912825 A 19891103**

Priority  
US 26746088 A 19881104

Abstract (en)  
[origin: WO9005334A1] A processor is disclosed for use in a computer system for comparing a number of bytes simultaneously in order to locate a particular character in a string of data. The processor includes a register (B) for holding the data bytes, a register (A) for storing the particular character, a comparison circuit (102, 109) for simultaneously comparing the bytes of the first register (B) with the bytes of the second register (A), and a circuit (115, 122) for generating indicator bits when a match has been found between the two registers. Microcode instructions cause the system to branch to a predetermined memory location when the control character has been located and to branch to a second predetermined memory location when no control character is found in the data string. A second portion of the processor finds the indicator bits generated from the circuit (115, 122) which have a predetermined characteristic and thus identifies the position of a particular byte in the data word that has the selected predetermined characteristic. In particular, four instructions are provided which find the first matching byte; the first non-matching byte; the first matching byte after the first non-matching byte; and the first non-matching byte after the first matching byte.

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**G06F 7/02**

IPC 8 full level  
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CPC (source: EP KR)  
**G06F 7/02** (2013.01 - EP KR); **G06F 7/74** (2013.01 - EP); **G06F 9/30018** (2013.01 - EP KR); **G06F 9/30038** (2023.08 - EP KR); **G06F 2207/025** (2013.01 - EP)

Citation (search report)  
• [Y] WO 8806308 A1 19880825 - DAVIN COMPUTER CORP [US]  
• [Y] Electronique Industrielle, No. 122, April 1969, pp259-265; A. LEJEUNE: "La mémoire passive à 128 bits et ses applications "SUR MESURE"  
• See also references of WO 9005334A1

Designated contracting state (EPC)  
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