Title (en)

PIXEL-DEPTH CONVERTER FOR A COMPUTER VIDEO DISPLAY

Publication

EP 0457039 A3 19920506 (EN)

Application

EP 91105970 A 19910415

Priority

US 52420190 A 19900516

Abstract (en)

[origin: EP0457039A2] A pixel-depth converter for converting source-pixel data having a source-pixel depth to destination-pixel data having a destination-pixel depth which differs from the source-pixel depth by a user-selectable pixel-depth-conversion scale factor includes a packed-pixel-data depacker circuit, a pixel-data-conversion-table storage circuit and a plurality of conversion-table address-selector multiplexers. The packed-pixel-data depacker circuit receives source-pixel data words having a packed-pixel data format from a source-pixel-data memory and transmits the data words depacked-pixel-data-word-component-by-depacked-pixel-data-word-component in accordance with the selected pixel-depth-conversion scale factor. The pixel-data-conversion-table storage circuit stores user-selectable depth-altering pixel-data-conversion data in locations having conversion-table read addresses which are associated with values of depacked-source-pixel-data portions corresponding to the selected pixel-depth-conversion scale factor. The pixel-data-conversion-table storage circuit includes a plurality of independently-operable converted-data-read parallel output ports and a like plurality of associated conversion-table read-address input ports. Depacked-source-pixel-data-portion conversion-lookup addresses may be applied independently in parallel to the plurality of conversion-table read-address input ports of the pixel-data-conversion-table storage circuit and pixel-data-conversion data stored in locations specified by the addresses can be read in parallel from the associated converted-data-read parallel output ports. Each conversion-table address-selector multiplexer has a plurality of depacked-source-pixel-data-portion input ports, a conversion-lookup address output port and an address-selector-multiplexer control-signal input port. The depacked-source-pixel-data-portion input ports of each address-selector multiplexer are connected respectively to corresponding terminal subsets of the depacker circuit which are associated with different pixel-depth-conversion scale factors. The conversion-lookup address output port of each of the conversion-table address-selector multiplexers is connected to an associated read-address input port of the pixel-data-conversion-table storage circuit. Finally, the address-selector-multiplexer control-signal input ports are connectable to a scale-factor-selection signal bus for receiving a scale-factor-selection signal which specifies the desired pixel-depth-conversion scale factor and corresponding depacked-source-pixel-data portions to serve as depacked-source-pixel-data-portion conversion-lookup addresses. <IMAGE>

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G09G 5/14

IPC 8 full level

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CPC (source: EP)

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Citation (search report)

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