

Title (en)  
Semiconductor memory cell.

Title (de)  
Halbleiterspeicherzelle.

Title (fr)  
Cellule de mémoire à semi-conducteurs.

Publication  
**EP 0460691 A2 19911211 (EN)**

Application  
**EP 91109338 A 19910607**

Priority  
JP 14854390 A 19900608

Abstract (en)  
Disclosed is a semiconductor memory cell comprising a word line (WL), a pair of bit lines (BL AND BL) crossing the word line (WL), a resistance (R1) of which the one side is connected to a high power source (VDD) and the other side to a first connecting node (M1), a first FET (FET1) connected between the first connecting node (M1) and a low power source (VSS) and of which the gate is connected to a second connecting node (M2), a second FET (FET2) connected between the second connecting node (M2) and the low power source (VSS) and of which the gate is connected to the first connecting node (M1), a third FET (FET3) connected between the first connecting node (M1) and one of the pair of bit lines (BL) and of which the gate is connected to the word line (WL) to control the operation of the third FET (FET3) by changing the potential of the word line (WL), and a fourth FET (FET4) connected between the second connecting node (M2) and the other of the pair of bit lines (BL) and of which the gate is connected to the word line (WL) to control the operation of the fourth FET (FET4) by changing the potential of the word line (WL). <IMAGE>

IPC 1-7  
**G11C 7/00; G11C 11/00; G11C 11/412; G11C 17/12**

IPC 8 full level  
**G11C 7/00** (2006.01); **G11C 7/20** (2006.01); **G11C 11/41** (2006.01); **G11C 11/412** (2006.01); **G11C 17/12** (2006.01); **H10B 10/00** (2023.01);  
**H10B 20/00** (2023.01)

CPC (source: EP KR US)  
**G11C 7/20** (2013.01 - EP US); **G11C 11/40** (2013.01 - KR); **G11C 11/412** (2013.01 - EP US); **G11C 17/12** (2013.01 - EP US)

Cited by  
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DOCDB simple family (publication)  
**EP 0460691 A2 19911211; EP 0460691 A3 19920429; EP 0460691 B1 19970108**; DE 69124010 D1 19970220; DE 69124010 T2 19970528;  
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