Title (en)

Integrated circuit with co-integrated power supply reduction

Title (de)

Integrierte Schaltung mit mitintegrierter Speisespannungsherabsetzung

Title (fr)

Circuit intégré à diminution intégrée de la tension d'alimentation

Publication

EP 0464909 B1 19960117 (EN)

Application

EP 91201582 A 19910620

Priority

NL 9001493 A 19900629

Abstract (en)

[origin: EP0464909A1] An integrated circuit has an internal supply voltage with a positive temperature coefficient, as a result of which the switching rate and the nuisance caused by "hot carrier stress" are less sensitive to temperature. <IMAGE>

IPC 1-7

G05F 1/625

IPC 8 full level

H02M 3/07 (2006.01); **G05F 1/625** (2006.01)

CPC (source: EP)

G05F 1/625 (2013.01)

Citation (examination)

Digest of the ESSCIRC 1987, pages 125 - 128; Sansen, Frank & Steyaert: "A New CMOS Current Reference"

Cited by

EP0896417A3

Designated contracting state (EPC)

DE FR GB IT

DOCDB simple family (publication)

EP 0464909 A1 19920108; **EP 0464909 B1 19960117**; DE 69116451 D1 19960229; DE 69116451 T2 19960808; JP 3299551 B2 20020708; JP H0549237 A 19930226; KR 100196592 B1 19990615; NL 9001493 A 19920116

DOCDB simple family (application)

EP 91201582 A 19910620; DE 69116451 T 19910620; JP 18287291 A 19910629; KR 910010639 A 19910626; NL 9001493 A 19900629