Title (en)

Microprocessor with multiple bus configurations.

Title (de)

Mikroprozessor mit einer Vielzahl von Buskonfigurationen.

Title (fr)

Microprocesseur avec plusieurs configurations de bus.

Publication

EP 0466970 A1 19920122 (EN)

Application

EP 90113991 A 19900720

Priority

EP 90113991 A 19900720

Abstract (en)

The invention relates to a microprocessor which consists of a processor unit (2) with an internal bus (4, 5, 6) and a programmable bus control unit (3) with an external bus (7, 8, 9). The bus control unit (3) interconnects the internal bus with the external bus via multiplexers latches and control logic. Thus, the following bus modes are programmable: 8-, and 16-bit multiplexed bus mode and 8-, and 16-bit non- multiplexed bus mode. The bus control unit (3) generates all necessary control signals adjusting their timing to the respective bus type. Via different control registers one can select different bus configurations for several address ranges. Furthermore, the timing of the bus signals is programable to allow slower peripherals to be connected to the microprocessor. <IMAGE>

IPC 1-7

G06F 13/40

IPC 8 full level

G06F 13/38 (2006.01); **G06F 13/40** (2006.01)

CPC (source: EP)

G06F 13/4018 (2013.01)

Citation (search report)
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Designated contracting state (EPC)

AT BE CH DE DK ES FR GB GR IT LI LU NL SE

DOCDB simple family (publication)

EP 0466970 A1 19920122; **EP 0466970 B1 20040922**; DE 69034165 D1 20041028; DE 69034165 T2 20050922; JP H04260959 A 19920916

DOCDB simple family (application)

EP 90113991 A 19900720; DE 69034165 T 19900720; JP 20253791 A 19910717