

Title (en)

GRAPHICS DISPLAY SYSTEM INCLUDING A VIDEO RANDOM ACCESS MEMORY WITH A SPLIT SERIAL REGISTER AND A RUN COUNTER

Publication

EP 0474366 A3 19921119 (EN)

Application

EP 91307222 A 19910806

Priority

- US 56346990 A 19900806
- US 56347290 A 19900806

Abstract (en)

[origin: EP0474366A2] A graphics system includes a random access memory (105) with a split serial register (109) having low and high halves of a plurality of storage elements, an access start point address register (137), and an arrangement (140, 142, 145) for stopping an access run at the end of a predetermined run length. Thus, there are specified both start and stop point addresses for a read data access operation from the split serial register in a graphics processing system. By using these start and stop point addresses, the operating speed of the graphics processing system is increased. The random access memory also includes a multiplexer (160) for coupling a column of storage cells from the memory array to storage elements of the split serial register (109). Data stored in either a low half or a high half of the addresses of the memory array may be selectively coupled through the multiplexer to either a low half or a high half of the split serial register. For a tile oriented graphics display operation, this arrangement increases the number of choices of where within the random access memory array to store specific bits of the tile data to be displayed. Data representing a tile can be mapped into a single row of the random access memory array. <IMAGE>

IPC 1-7

G09G 1/16

IPC 8 full level

G06T 1/60 (2006.01); **G09G 5/00** (2006.01); **G09G 5/36** (2006.01); **G09G 5/395** (2006.01)

CPC (source: EP)

G09G 5/395 (2013.01)

Citation (search report)

- [XP] EP 0398511 A2 19901122 - IBM [US]
- [A] US 4825411 A 19890425 - HAMANO HISANORI [JP]

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